

FIG. 1

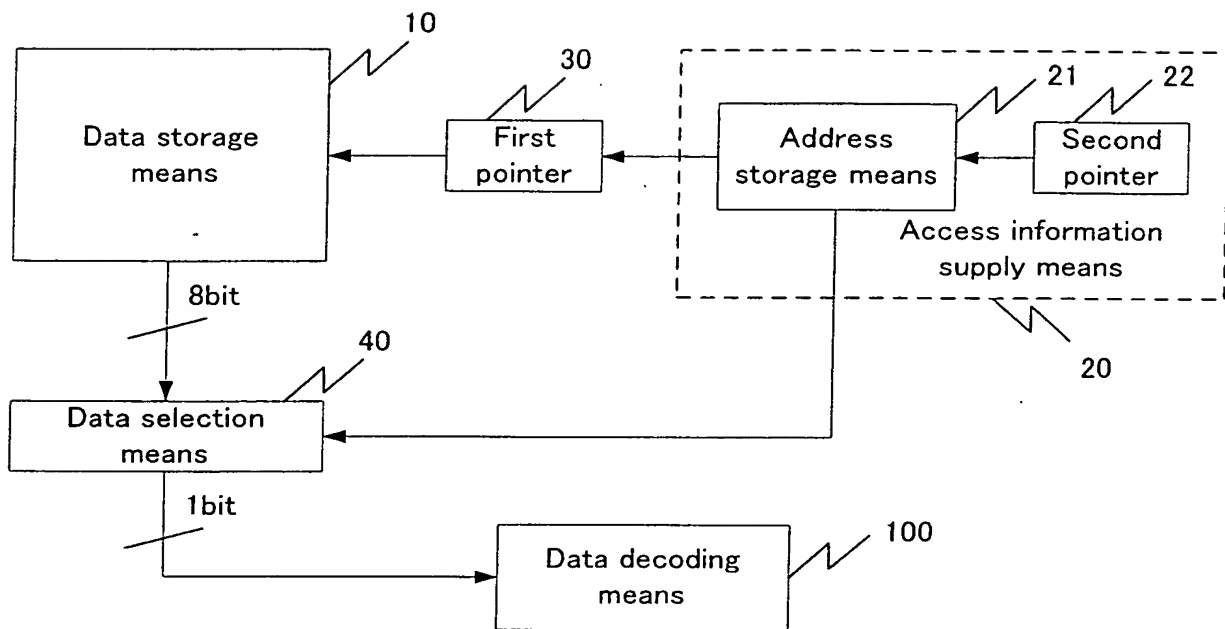


FIG. 2

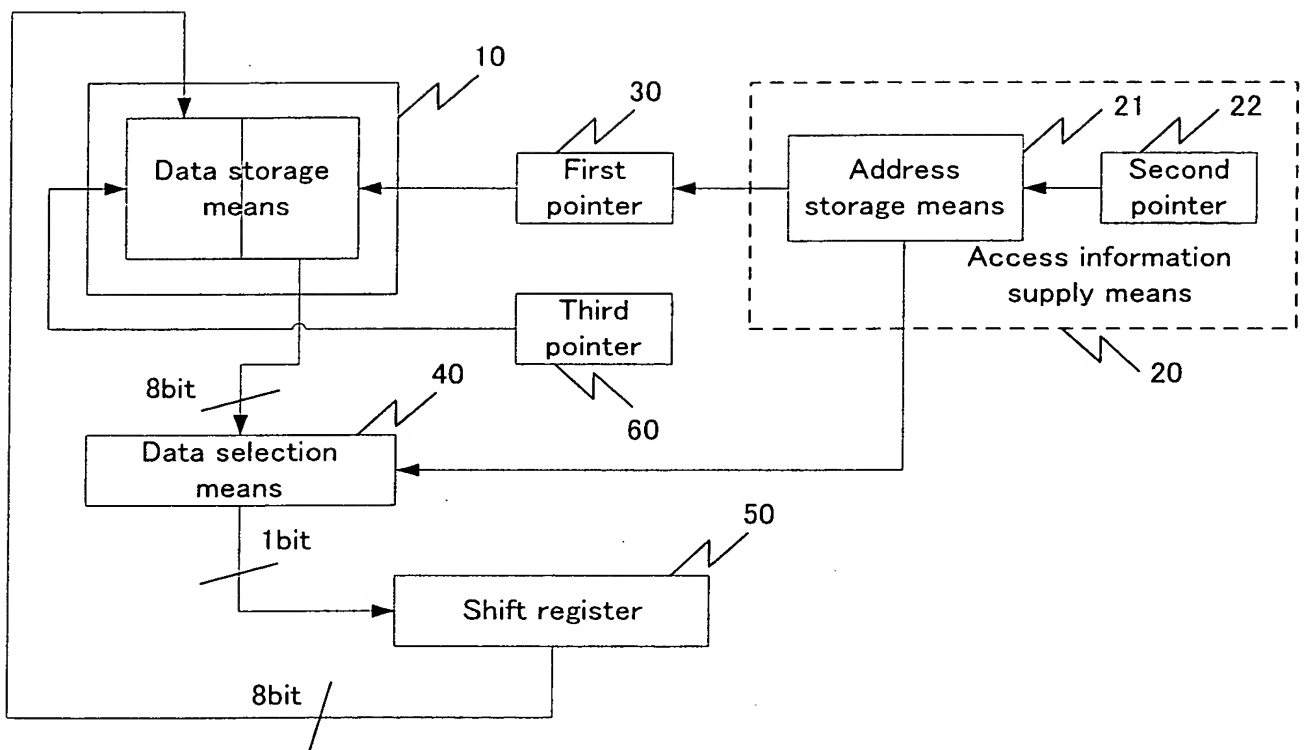


FIG. 3

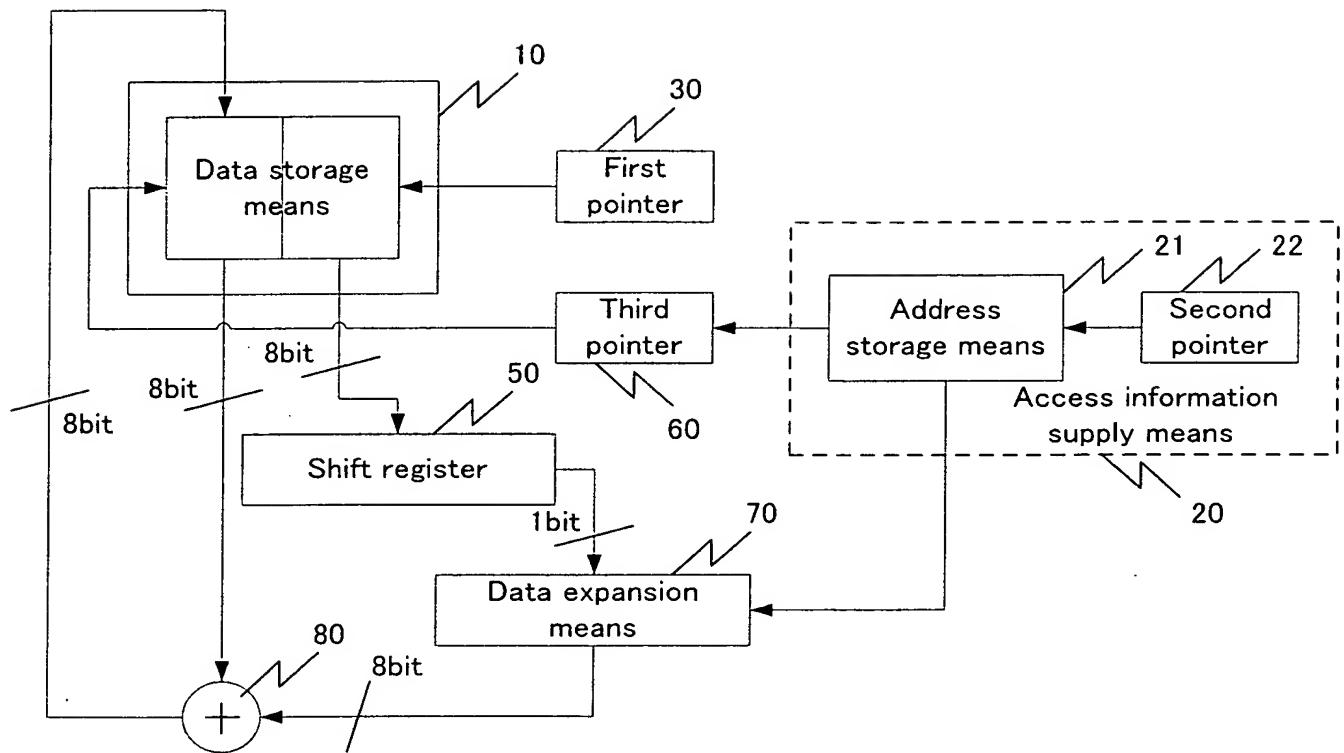


FIG. 4

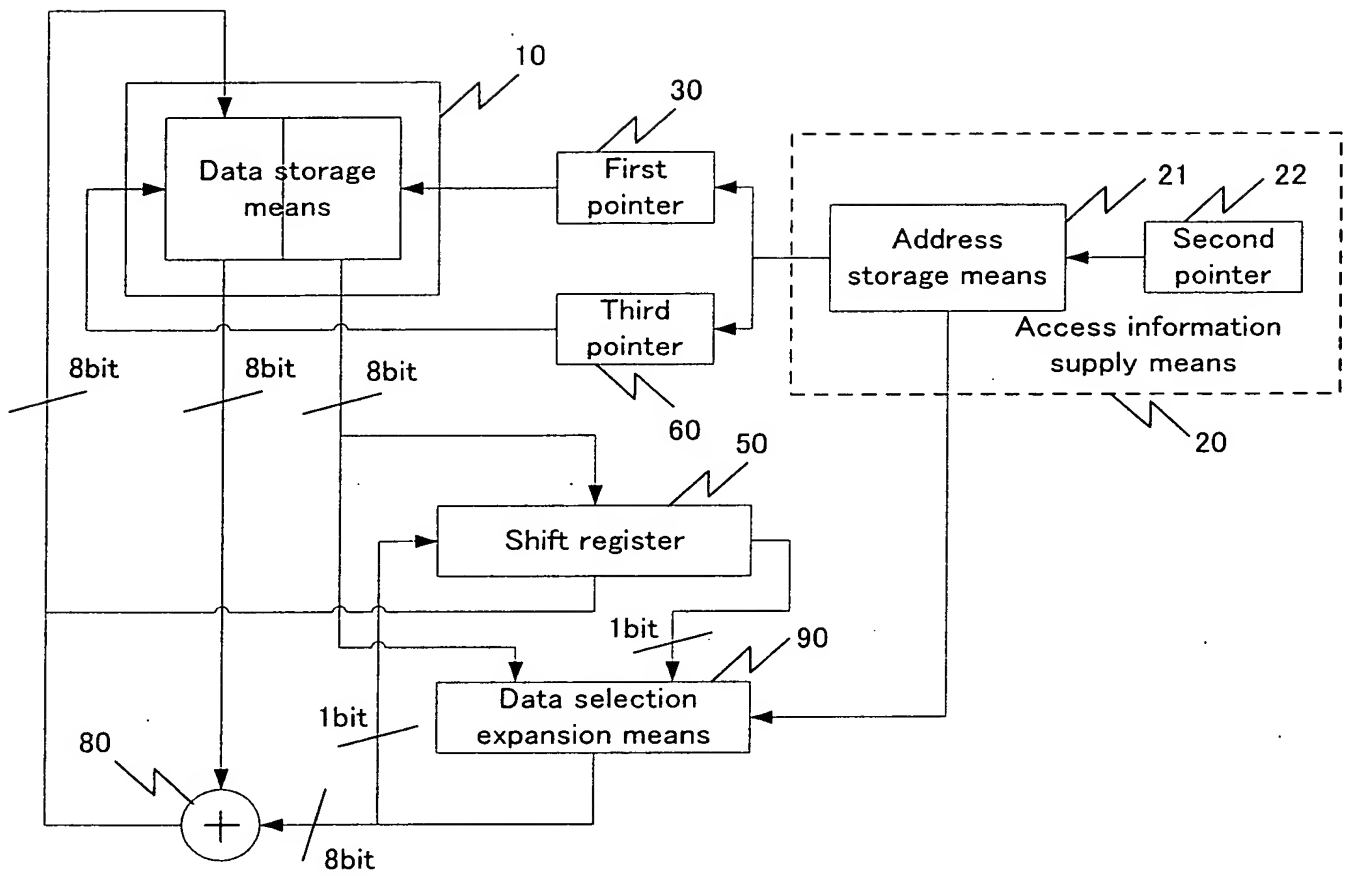


FIG. 5

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
100	d0	d1	d2	d3	d4	d5	d6	d7
101	d8	d9	d10	d11	d12	d13	d14	d15
102	d16	d17	d18	d19	d20	d21	d22	d23
103	d24	d25	d26	d27	d28	d29	d30	d31
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
300	d0	d4	d8	d12	d16	d20	d24	d28
301	d1	d5	d9	d13	d17	d21	d25	d29
302	d2	d6	d10	d14	d18	d22	d26	d30
303	d3	d7	d11	d15	d19	d23	d27	d31

FIG. 6

Address		Address information	Bit position information
0		100	bit7
1		100	bit3
2		101	bit7
3		101	bit3
4		102	bit7
5		102	bit3
6		103	bit7
7		103	bit3
8		100	bit6
⋮		⋮	⋮

FIG. 7

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
100	d0	d1	d2	d3	d4	d5	d6	d7
101	d8	d9	d10	d11	d12	d13	d14	d15
102	d16	d17	d18	d19	d20	d21	d22	d23
103	d24	d25	d26	d27	d28	d29	d30	d31
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
300	d0	d8	d16	d24	d1	d9	d17	d25
301	d2	d10	d18	d26	d3	d11	d19	d27
302	d4	d12	d20	d28	d5	d13	d21	d29
303	d6	d14	d22	d30	d7	d15	d23	d31

FIG. 8

Address		Address information	Bit position information
0		100	bit7
1		101	bit7
2		102	bit7
3		103	bit7
4		100	bit6
5		101	bit6
6		102	bit6
7		103	bit6
8		100	bit5
⋮		⋮	⋮

FIG. 9

Address		Address information	Bit position information
0		300	bit7
1		301	bit7
2		302	bit7
3		303	bit7
4		300	bit6
5		301	bit6
6		302	bit6
7		303	bit6
8		300	bit5
⋮		⋮	⋮

FIG. 10

Address		Address information	Bit position information
0		300	bit7
1		300	bit3
2		301	bit7
3		301	bit3
4		302	bit7
5		302	bit3
6		303	bit7
7		303	bit3
8		300	bit6
⋮		⋮	⋮

FIG. 11

Step	Processing
step0	First pointer 30 \leftarrow address information Second pointer 22 \leftarrow second pointer 22 + 1
step1	Setting of the number of repetitions
step2	Shift register 50 \leftarrow selection of specific bit of 1-word data stored in data storage means 10 (at address designated by first pointer 30) First pointer 30 \leftarrow address information Second pointer 22 \leftarrow second pointer 22 + 1 Return to step 2
step3	Data storage means 10 (at address designated by third pointer 60) \leftarrow shift register 50 Third pointer 60 \leftarrow third pointer 60 + 1
Step4	Return to step 1

FIG. 12

Step	Processing
step0	Setting of the number of repetitions (1) Third pointer 60 \leftarrow head address of processed data storage area
step1	Data storage means 10 (at address designated by third pointer 60) \leftarrow 'x'00 Third pointer 60 \leftarrow third pointer 60 + 1 Return to step 1
step2	Third pointer 60 \leftarrow address information Second pointer 22 \leftarrow second pointer 22 + 1
step3	Shift register 50 \leftarrow 1-word data stored in data storage means 10 (at address designated by first pointer 30) First pointer 30 \leftarrow first pointer 30 + 1
step4	Setting of the number of repetitions (2)
step5	Data storage means 10 (at address designated by third pointer 60) \leftarrow Setting of data element output from shift register in specific bit of 1-word data stored in data storage 10 (at address designated by third pointer 60) Third pointer 60 \leftarrow address information Second pointer 22 \leftarrow second pointer 22 + 1 Return to step 5
step6	Return to step 3

FIG. 13

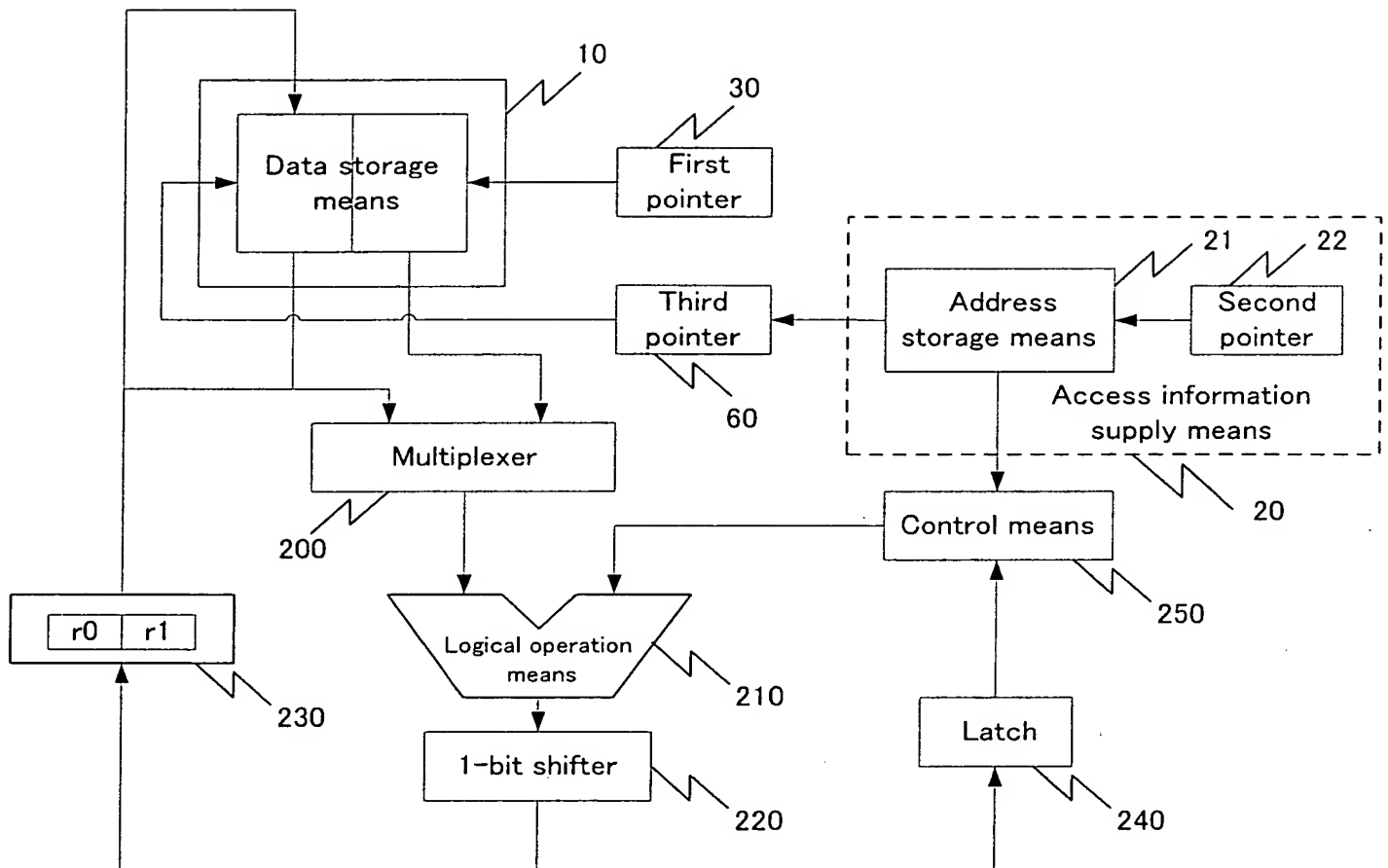


FIG. 14

Step	Processing
step0	Third pointer 60 \leftarrow address information
step1	r1 \leftarrow data storage means 10 (at address designated by first pointer 30) First pointer 30 \leftarrow first pointer 30 + 1
step2	Setting of the number of repetitions
step3	r0 \leftarrow setting of flag of latch 240 in specific bit of 1-word data stored in data storage means 10 (at address designated by third pointer 60) Second pointer 22 \leftarrow second pointer 22 + 1
step4	Data storage means 10 (at address designated by third pointer 60) \leftarrow r0
step5	r1 \leftarrow shifting of data in r1 to higher-order bits by one bit Third pointer 60 \leftarrow address information Return to step 3
step6	Return to step 1